F2

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
7 September 2001 (07.09.2001)

PCT

(10) International Publication Number
WO 01/65315 A2

(51) International Patent Classification[7]: G03F

(21) International Application Number: PCT/US01/06144

(22) International Filing Date: 26 February 2001 (26.02.2001)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
09/514,551 28 February 2000 (28.02.2000) US

(71) Applicant (*for all designated States except US*): NUMERICAL TECHNOLOGIES, INC. [US/US]; 70 West Plumeria Drive, San Jose, CA 95134-2134 (US).

(72) Inventors; and
(75) Inventors/Applicants (*for US only*): PIERRAT, Christophe [FR/US]; Apt. 307, 420 Riverside Court, Santa Clara, CA (US). ZHANG, You-Ping [CN/US]; 37151 Magnolia Street, Newark, CA 94560 (US). CHANG, Fang-Cheng [US/US]; 1361 Yukon Terrace, Sunnyvale, CA 94087 (US). PARK, Ho, Yong [KR/US]; 1035 Aster Ave. #2160, Sunnyvale, CA 94086 (US). WANG, Yao-Ting [—/US]; 970 Corte Madera Avenue, Sunnyvale, CA 94086 (US).

(74) Agent: JOHANSEN, Dag; Stattler Johansen & Adeli LLP, P.O. Box 51860, Palo Alto, CA 94303-0728 (US).

(81) Designated States (*national*): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CR, CU, CZ, DE, DK, DM, DZ, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZW.

(84) Designated States (*regional*): ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).

Published:

without international search report and to be republished upon receipt of that report

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: METHOD AND APPARATUS FOR MIXED-MODE OPTICAL PROXIMITY CORRECTION

(57) Abstract: A semiconductor layout testing and correction system is disclosed. The system combines both rule-based optical proximity correction and model-based optical proximity correction in order to test and correct semiconductor layouts. In a first embodiment, a semiconductor layout is first processed by a rule-based optical proximity correction system and then subsequently processed by a model-based optical proximity correction system. In another embodiment, the system first processes a semiconductor layout with a rule-based optical proximity correction system and then selectively processes difficult features using a model-based optical proximity correction system. In yet another embodiment, the system selectively processes the various features of a semiconductor layout using a rule-based optical proximity correction system or a model-based optical proximity correction system.

WO 01/65315 A2

METHOD AND APPARATUS FOR MIXED-MODE OPTICAL PROXIMITY CORRECTION

FIELD OF THE INVENTION

The present invention relates to the field of electronic semiconductor design and manufacture. In particular the present invention discloses methods for performing optical proximity correction.

BACKGROUND OF THE INVENTION

Semiconductor manufacturers produce semiconductors using optical lithography. Optical lithography is a specialized printing process that puts detailed patterns onto silicon wafers. Semiconductor manufacturers create a "mask" and then shine light through the mask to project a desired pattern onto a silicon wafer that is coated with a very thin layer of photosensitive material called "resist." The bright parts of the image pattern cause chemical reactions that make the resist material become soluble. After development, the resist forms a stenciled pattern across the wafer surface that accurately matches the desired pattern of the semiconductor circuit. Finally, this pattern is transferred onto the wafer surface via another chemical process.

To improve semiconductor performance, semiconductor researchers and engineers keep shrinking the size of the circuits on semiconductor chips. There are two main reasons to reduce the size of semiconductor circuits: (1) smaller features allow silicon chips to contain more circuit elements and thus be more complex. Similarly, a smaller circuit size allows more copies of the same die to appear on a single silicon wafer. (2) smaller circuit devices use less power and may operate at higher frequencies (faster rates) to produce higher performance semiconductor chips.

As semiconductor circuit sizes have reduced, the limits of optical lithography are being tested. However, the move to new semiconductor processes such as X-ray lithography is viewed as difficult and expensive. To extend the use of optical lithography into feature sizes that are smaller than the light wavelength used in the optical lithography process, a set of sub-wavelength techniques have been developed. Two sub-wavelength technologies that have been developed include phase-shifting and optical proximity correction. Phase shifting utilizes optical interference to improve depth-of-field and resolution in lithography. Optical proximity correction alters the original layout mask to compensate for nonlinear distortions caused by optical diffraction and resist process effects. Optical proximity correction may also correct for

mask proximity effects, dry etch effects, and other undesirable effects of the optical lithography process.

Optical proximity correction is often performed by modeling the final manufactured output of a semiconductor design and then determining what changes should be made to the semiconductor layout design to obtain a desired result. The semiconductor process modeling produces very accurate results. However, the semiconductor process modeling is extremely computationally expensive. Furthermore, adjusting a semiconductor layout design using model-based optical proximity correction is a very laborious task. It would be desirable to have a method of using optical proximity correction that produces good results within a short amount of time and reduce human intervention.

SUMMARY OF THE INVENTION

A semiconductor layout testing and correction system is disclosed. The system combines both rule-based optical proximity correction and model-based optical proximity correction in order to test and correct semiconductor layouts. In a first embodiment, a semiconductor layout is first processed by a rule-based optical proximity correction system and then subsequently processed by a model-based optical proximity correction system. In another embodiment, the system first processes a semiconductor layout with a rule-based optical proximity correction system and then selectively processes difficult features using a model-based optical proximity correction system. In yet another embodiment, the system selectively processes the various features of a semiconductor layout using a rule-based optical proximity correction system or a model-based optical proximity correction system.

Other objects, features, and advantages of present invention will be apparent from the company drawings and from the following detailed description.

BRIEF DESCRIPTION OF THE DRAWINGS

The objects, features, and advantages of the present invention will be apparent to one skilled in the art, in view of the following detailed description in which:

Figure 1A illustrates an ideal mask of a geometric pattern.

Figure 1B illustrates a mask of the ideal geometric pattern of **Figure 1A.**

Figure 1C illustrates a circuit element created in the photoresist of a silicon wafer using the mask of **Figure 1B.**

Figure 2A illustrates an optical proximity corrected version of the ideal geometric pattern of **Figure 1A.**

Figure 2B illustrates an optical proximity corrected photomask of the optical proximity corrected version of the ideal geometric pattern illustrated in **Figure 2A.**

Figure 2C illustrates a circuit element created in the photoresist of a silicon wafer using the photomask of **Figure 2B.**

Figure 3A illustrates an ideal rectangular geometric feature.

Figure 3B illustrates a circuit element created in the photoresist of a silicon wafer using the photomask of **Figure 3A.**

Figure 3C illustrates the rectangular geometric feature of **Figure 3A** after it has been processed by a rule-based optical proximity corrector that adds serifs to outside corners.

Figure 3D illustrates a circuit element created in the photoresist of a silicon wafer using the optical proximity corrected photomask of **Figure 3C.**

Figure 4A illustrates two close geometric features that have closely parallel feature lines.

Figure 4B illustrates the geometric features of **Figure 4A** after enlarging the gap between the two features.

Figure 5 conceptually illustrates the modeling of the optical lithography process.

Figure 6A illustrates the layout of an ideal rectangular geometric feature that has had its segments subdivided.

Figure 6B illustrates a circuit element created in the photoresist of a silicon wafer using the photomask of **Figure 6A**.

Figure 6C illustrates the rectangular geometric feature of **Figure 6A** after two segments in the upper-right corner have been adjusted using model-based optical proximity correction.

Figure 6D illustrates a circuit element created in the photoresist of a silicon wafer using the optical proximity adjusted photomask of **Figure 6C**.

Figure 7 illustrates a flow diagram of an optical proximity correction system that uses both rule-based optical proximity correction and model-based optical proximity correction.

Figure 8 illustrates a flow diagram of an optical proximity correction system that applies rule-based optical proximity correction and then selectively applies model-based optical proximity correction.

Figure 9 illustrates a flow diagram of an optical proximity correction system that selectively applies rule-based optical proximity correction or model-based optical proximity correction to various layout features.

Figure 10 illustrates a conceptual diagram of an optical proximity correction system that selectively applies rule-based optical proximity correction, model-based optical proximity correction, rule-based and model-based optical proximity correction, or no correction to various layout features.

Figure 11A illustrates a detailed flow diagram for one embodiment of the optical proximity correction system that selectively applies rule-based optical proximity correction, model-based optical proximity correction, rule-based and model-based optical proximity correction, or no correction to various layout features as set forth in **Figure 10**.

Figure 11B illustrates a legend for the flow diagram of **Figure 11A**.

Figure 12 illustrates a computer system that may embody the teachings of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

A method and apparatus for mixed-mode optical proximity correction is disclosed. In the following description, for purposes of explanation, specific nomenclature is set forth to provide a thorough understanding of the present invention. However, it will be apparent to one skilled in the art that these specific details are not required in order to practice the present invention. For example, the present invention has been described with reference to optical lithography. However, the same techniques can easily be applied to other types of semiconductor processes such as X-ray lithography, Extreme UV lithography, electron beam manufacturing, and focused ion beam manufacturing.

Optical Proximity Correction

Semiconductor manufacturers are reaching the limits of optical lithography using visible light wavelengths. **Figures 1A** through **1C** illustrate an example of the difficulties of using optical lithography to create small features that are smaller than the light wavelength used in the lithography processes. **Figure 1A** illustrates an ideal pair of geometric features to be etched into a silicon wafer. When a photomask is created, the photomask is not a perfect representation of the ideal geometric feature. For example, **Figure 1B** illustrates a photomask of the ideal geometric features illustrated in **Figure 1A**.

When the photomask of **Figure 1B** is used in the optical lithography process, the final output silicon may appear as illustrated in **Figure 1C**. Note that the outside corners **160** of the final output features become have become shortened and rounded. Similarly, the inside corner **150** has become rounded and occupies more space than desired. Thus, the output features of **Figure 1C** only appear roughly similar to the ideal output features of **Figure 1A**.

To extend the use of optical lithography to create geometric features that are smaller than the light wavelength used in the optical lithography process, a set of sub-wavelength techniques have been developed. Optical proximity correction is one of those sub-wavelength techniques. Optical proximity correction is the process of altering the original mask to compensate for nonlinear distortions caused by optical diffraction and photoresist process effects.

Figures 2A through **2C** illustrate how optical proximity correction can be used to improve the optical lithography process to create a better version of the features illustrated in **Figures 1A** through **1C**. Referring to **Figure 2A**, the ideal geometric feature layout of **Figure**

1A has been altered to compensate for optical diffraction and other effects. As illustrated in **Figure 2A**, a serif has been added to the outside corners to provide extra area that reduce diffraction effects. Similarly, the inside corner **210** has area removed. When a photomask of the optical proximity corrected version is created, it may appear as illustrated in **Figure 2B**. When the optical proximity corrected photomask of **Figure 2B** is used within the optical lithography process to create a silicon semiconductor, the output circuit features may appear as illustrated in **Figure 2C**. As can be seen from the drawings, the optical proximity corrected output circuit illustrated in **Figure 2C** more accurately resembles the desired geometric features of **Figure 1A** that the uncorrected output circuit of **Figure 1C**.

There are two main methods of performing optical proximity correction: rule-based optical proximity correction and model-based optical proximity correction. Each method has its own advantages and disadvantages.

Rule-Based Optical Proximity Correction

A first method of performing optical proximity correction is to create and apply a set of optical proximity correction rules. Each optical proximity correction rule tests for a particular condition wherein optical proximity correction may be necessary. To illustrate how rule-based optical proximity correction operates, a couple of sample optical proximity correction rules are provided:

If an outside corner is detected then add a serif to provide extra area around the corner.

If a feature line from a first object is very closely parallel to another feature line of a second object then move the feature line of the wider of the two objects away from the other feature line.

These are only two example rules; many other different rules exist or may be subsequently created. Rules are often generated offline by way of simulation for very typical and general patterns. It is possible that different features are mistakenly characterized as the same such that an inaccurate correction is performed.

The first rule is illustrated with reference to **Figures 3A, 3B, 3C,** and **3D**. Referring to **Figure 3A**, a geometric feature has four corners. Due to light diffraction around the corners of the mask pattern in **Figure 3A**, the resultant feature in the photoresist appears as illustrated in **Figure 3B**. To counteract this effect, a serif has been added around the corner of the mask as

illustrated in **Figure 3C**. The end-result is an improved end-result geometric feature as illustrated in **Figure 3D**.

The second rule ensures that adjacent parallel feature lines are not too close. **Figure 4A** illustrates two adjacent geometric objects **450** and **460** that have very close parallel lines separated by the space **410**. When parallel features are so close, the manufactured features may appear too close as illustrate in **Figure 4B**. To prevent such features from being manufactured too close to each other, the space **410** between geometric objects **450** and **460** should be increased. **Figure 4C** illustrates two features after the space **415** between the geometric features **455** and **465** has been widened. The rule selects the wider of the two objects (object **450**) and moves its parallel adjacent feature line away from the other object (object **460**). The final manufactured result is illustrated in **Figure 4D**.

Rule-based optical proximity correction has the advantage that it is relatively simple to apply once a set of optical proximity correction rules have been defined. No very complex calculations are required to improve the final layout. A rule engine simply attempts to apply each rule to each feature of a proposed layout. However, the rules-based optical proximity correction system is rigid in that only problems that have associated rules are handled. Furthermore, the number of rules can grow exponentially as smaller and smaller processes are used. This is especially true when the features size is much smaller than the range of the proximity effect. It is very difficult to maintain such large rule sets. Since each layout change effects the entire nearby region, it is difficult to create rules when the light wavelength exceeds the features size.

Model-Based Optical Proximity Correction

Model-based optical proximity correction operates using a mathematical model of the manufacturing process. The mathematical model of the manufacturing process accurately determines how the output circuit pattern would appear if a given photomask layout pattern was put through that particular manufacturing process. It should be noted that many different models are created for many different manufacturing process. Each manufacturing process may have more than one different type of model. For an optical lithography processes, the model may handle effects such as mask fabrication effects, optical effects, resist processing effects, dry or wet etching effects, or other effects of the optical lithography process.

Figure 5 conceptually illustrates the model-based optical proximity correction process. Referring to **Figure 5**, circuit designers work with electronic design tools to create a layout pattern **510**. An optical lithography model **520** is then applied to the input layout pattern **510** to simulate the optical lithography process. The optical lithography model **520** produces an output-modeled circuit **550**. One type of optical lithography model is a convolution model. Current optical lithography convolution models are very accurate such that the output-modeled circuit produced by the optical lithography convolution model is almost exactly like the real circuit output from an actual optical lithography process.

By examining the output modeled circuit pattern from an optical lithography convolution model, trouble spots can be located. The source areas of the pattern mask that created the trouble spots can then be adjusted. Typically, reference points on the output circuit pattern are selected and specified to be located at a certain defined location within a designated threshold tolerance. Then, the related feature of the input layout pattern is adjusted until the reference point of the output circuit pattern falls within the designated threshold of the defined location.

One method of performing model-based optical proximity correction is to divide each feature into many sub segments and adjust each individual sub segment to obtain the desired resultant feature. An example of this is provided with reference to **Figures 6A, 6B, 6C**, and **6D**. **Figure 6A** illustrates an example rectangular feature that normally has four segments. However, to carefully adjust how the output circuit device will appear, each of the four segments has been sub-divided into three smaller segments. **Figure 6B** illustrates the normal output of the rectangular feature of **Figure 6A.**

To correct the shortening and rounding of the upper-right corner, segment **610** and segment **620** may be moved out to provide more area. An example of this is illustrated in **Figure 6C** wherein segment **610** has been moved up to create segment **615** and segment **620** has been moved right to create segment **625**. Note that the endpoints of the moved segments will remain coupled to the unmoved segments using additional segments to connect the endpoints. Thus, a newly created horizontal segment will couple segment **625** and unmoved segment **630** in **Figure 6C**. **Figure 6D** illustrates how the improved output wherein the upper right-hand corner **690** is less rounded. Through simulation, it may be found that by moving segments **610** and **620** out by a certain amount, light intensity at the evaluation points gets gradually closer and eventually meets a target threshold. Since the evaluation point is chosen such that it well represent the behavior when printed, we can conclude that the printing will meet the specified target with the

specified edge movement. Note that this process completes a verification process for this particular segment.

Model-based optical proximity correction is a very powerful tool for ensuring that a fabricated circuit operates as desired since it can be used to verify that all the created circuit features meet the minimum requirements. However, this power comes at a cost. To use model-based optical proximity correction across an entire complex design requires many hours of computation time. For many projects, having a fast turn-around time is very important. It would therefore be desirable to have methods that produces the accuracy of model-based optical proximity correction without requiring such a large amount of time for computations.

Mixed Mode Optical Proximity Correction

To perform optical proximity correction in a time-efficient manner that produces functional results, the present invention introduces a mixed-mode system of optical proximity correction. Specifically, the present invention introduces several methods of combining the two different methods of performing optical proximity correction such that very good results can be achieved in short amount of time.

Rule Based OPC then Model Based OPC

In a first embodiment, a rule-based optical proximity correction system parses through a semiconductor layout to perform a first pass optical proximity correction and then a model-based optical proximity correction system is used to cure any remaining trouble spots. A sample implementation is illustrated in **Figure 7**.

Referring to **Figure 7**, a first step **720** applies a set of optical proximity correction rules to the semiconductor layout. The rules used in step **720** modify the layout in attempts to correct certain problems that can be located by identifying specific conditions in the layout. However, there are layout problems that are not easily identified with a rule.

Next, at step **730**, the system applies a lithography model to the semiconductor to determine how the manufactured output of the current layout would appear. At step **740**, the system tests the modeled output to determine if the manufactured output from the layout conforms to a designated specification. If no problem is detected, the system proceeds to step **770** to output a final semiconductor layout.

If a layout problem is detected, the system proceeds to step **750** to correct the problem using the model-based optical proximity correction system. In one embodiment, a model-based OPC system determines the outcome of two different feature placements and then interpolates an idea position between the two placements. A number of different identified problems may be addressed during step **750**. The system then proceeds to again check the layout with manufacturing model at step **730**. This process iterates until no more significant problems are detected at step **740**. Once no significant problems are detected at step **740** the system outputs a final semiconductor layout at step **770**.

The method illustrated in **Figure 7** provides advantages over rule-based OPC or model-based OPC alone. The system provides a better output layout than rule-based OPC alone since the model-based OPC portion handles many situations that are not handled easily using rule-based OPC. Furthermore, the system may be faster than model-based OPC alone since many layout problems are quickly solved using rule-based OPC such that model-based OPC may not be needed in many situations. Furthermore, it should be noted that the entire design is validated using model-based OPC such that the system creates layouts that are just as good as model-based OPC corrected only layouts but in less time since the rule-based OPC corrects many problems that are easily identified using rule-based OPC.

Rule-Based OPC and Selective Model-Based OPC

In other embodiments of the present invention, a rule-based proximity correction system and a proximity correction system are selectively used depending on the situation. Various different embodiments of this technique have been implemented.

Figure 8 illustrates a first embodiment of a selective optical proximity correction system wherein the rules-based OPC is used for all features, but the model-based OPC is selectively used. Referring to step **820** the system applies a set of optical proximity correction rules to the semiconductor layout. The rules correct a number of problems that can easily be identified using a set of rules. The rules may be created using multiple different models. For example, clear field patterns could be fitted better using one model and dark field patterns may be fitted better using another model.

At step **830**, the system enters a loop that begins to examine every feature in the layout to determine if model-based optical proximity correction should be applied to that feature. The

system may look for certain features where layout problems that cannot be easily corrected using a rule. The features that need model based OPC are marked at step **830**.

At step **830**, the system breaks down all the features identified for model-based OPC. The feature break down may occur as illustrated in **Figure 6A** where a geometric feature has been divided into sub segments. By determining if a particular segment falls within a certain situation, the present invention will determine if the segment should be processed by a model-based optical proximity correction system. A set of defined rules can be used to make such determinations. For example, the following three rules may specify situations wherein model-based optical proximity correction may be advisable:

1. If a segment forms portion of an outside corner then process the segment with a model-based optical proximity correction system.
2. If a segment forms an edge of a narrow feature then process the segment with a model-based optical proximity correction system.
3. If a segment forms an edge that is closely parallel to a neighboring feature then process the segment with a model-based optical proximity correction system.

These are only examples of decision rules that may be used to determine if model-based optical proximity correction should be used.

Referring back to **Figure 8**, at step **850** the system determines the outcome of the rule tests. If the segment fell within one of the conditions defined in a rule, then the system examines and corrects the segment using model-based optical proximity correction at step **840**. The system then proceeds to the next segment at step **830**.

After examining a feature to determine if it falls within one of conditions wherein model-based optical proximity correction is required, the system proceeds from step **830** to step **840** where it determines if this was the last feature to examine. If the examined feature was not the last feature then the system proceeds back to step **830** to examine the next feature. Once all the features have been tested, the system may optionally pre-bias the marked features at step **850**. However, it is not likely that the pre-bias is needed in this case since all the edges have been pre-corrected using rules-based OPC.

After pre-biasing (if done), the system applies a lithography model to the layout at step **860** to determine how the manufactured output of the current layout would appear. At step **870**,

the system tests the modeled output to determine if the manufactured output from the layout conforms to a designated specification. If no problem is detected, the system proceeds to step **890** to output a final semiconductor layout.

If one or more layout problems are detected, the system proceeds to step **880** to correct the problems using the model-based optical proximity correction system. The system then proceeds to again check the layout with manufacturing model at step **860**. This process iterates until no more significant problems are detected at step **870**. Once no significant problems are detected at step **870** the system outputs a final semiconductor layout at step **890**.

The system of **Figure 8** allows rule-based optical proximity correction to correct many easily identified problems but then uses model-based optical proximity correction to carefully handle features in difficult situations. Thus, the system of **Figure 8** produces a high quality semiconductor layout without requiring the computation time of a full model-based optical proximity correction pass. The system of **Figure 8** will be significantly faster than a normal model-based OPC system since model-based OPC is not applied to every feature.

<u>Selective Rule-Based OPC or Model-Based OPC</u>

Figure 9 illustrates another embodiment of a selective optical proximity correction system. In the system of **Figure 9**, features are selectively processed using rule-based OPC or model-based OPC but not both.

The embodiment of **Figure 9** begins as a loop that examines each feature. First, at step **910** each feature is tested with a set of selective rules that determine if rule-based optical proximity correction or model-based optical proximity correction should be used on that feature. The same set of rules as defined in the previous section may be used. Note that the selective rules are designed to safeguard the rule correction areas to ensure that the rule correction actually will meet the specification. Thus, such features can skip the performance check or model-based OPC. The determination at step **920** marks each feature to be model-based OPC correct at step **925** or to be rule-based OPC correct at step **930**. This process is repeated for all features using the decision step at step **940**.

At step **950** the system invokes rule-based optical proximity correction to correct all the features marked for rule based OPC at step **930**. Those features marked for model-based OPC are not examined.

At step **960**, the system may optionally pre-bias the features marked for model-based optical proximity correction. The pre-bias may be a set of rules in which the pattern is defined solely by the feature shape itself and the surrounding environment is ignored.

A step **970**, the system tests the features marked for model-based OPC with a model of the manufacturing process. If all features are to specification at step **980**, then the system outputs a final semiconductor layout at step **990**. Otherwise, the features marked for model-based OPC are corrected using model-based OPC at step **985**.

<u>Selective Rule-Based OPC, Model-Based OPC, Rule and Model OPC or No Correction</u>

Figure 10 illustrates a conceptual diagram of yet another possible embodiment of a selective OPC system. In the system of **Figure 10**, each the features may be adjusted using rule-based OPC, model-based OPC, rule and model based OPC, or no correction at all.

Referring to the conceptual diagram of **Figure 10**, the first step is to process the layout to put it in a form where it may be tested using a set of correction type selection rules. As indicated in step **1010**, this may be performed by dividing the layout into individual segments and setting evaluation points. However, other systems may be used.

Next, at step **1020**, all of the segments are examined and divided into different sets wherein each set will have a different OPC correction system used. Some segments will be placed into a set where no correction (NC) is needed. A second set of segments will then be placed into a set wherein only rule-based correction (RC) will be applied. A third set of segments will then be placed into a set wherein only model-based correction (MC) will be applied. Finally, a fourth set of segments will be placed into a set that will use both rule and model based correction (RMC).

The system will then process each set of segments accordingly. The segments that require no correction will be placed directly into the output. The segments that require rule-based correction (RC) or rule and model based correction (RMC) segments will be processed using rule-based correction at step **1030**. The rule-based correction only (RC) segments will then be placed into the output as set forth in step **1040**.

The model-based correction only (MC) segments may be pre-biased at step **1050**. Finally, the model-based correction only (MC) segments and the rule and model based correction (RMC) segments are processed using model-based OPC at step **1060**.

Figure 11A illustrates a detailed flow diagram describing one implementation of the selective OPC system of **Figure 10**. The embodiment of **Figure 11A** has been described with reference to an edge based system. However, the same teachings can be applied to other types of systems such as a shape based correction system. **Figure 11A** has been illustrated with three different line types. A legend for the different dataflow types is provided in **Figure 11B**.

Referring to **Figure 11A**, the system begins with an original layout **1102**. From the original layout **1102**, the system builds a correctable edge database **1107** at step **1105**. Note that a correctable edge database does not have to explicitly be created and maintained in all embodiments. For example, one embodiment may explicitly derive the edges from the layout database **1102** on the fly. The system then proceeds to examine all the edges in the correctable edge database **1107** to determine which type of correction should be used on each edge. At step **1110**, the system extracts an edge from the correctable edge database **1107** and tests that edge at step **1115**. If no correction is required the system proceeds back to step **1110** to examine another edge.

If the edge needs rule-based OPC (**RC**) or rule and model based OPC (**RMC**) then the system proceeds to step **1120** to apply the rules **1125**. Note that rule-based correction can be performed on an edge by edge basis. If the edge required only rule-based OPC (**RC**) then the system applies the correction to the layout database as specified in step **1135** before returning to step **1110** to examine another edge. If the edge requires rule and model based OPC (**RMC**) then the system proceeds to step **1140** to initialize the edge with the correction from the rule. That corrected edge is then used to update a model-based OPC edge database **1147** at step **1145**. After updating the model-based OPC edge database **1147**, the system proceeds back to step **1110** to examine another edge.

Referring back to step **1110**, if the edge requires model-based OPC only (**MC**), then the system proceeds to step **1150** where the system may pre-bias the edge. Then, the system updates the model-based OPC edge database **1147** at step **1145** with that pre-biased edge. After updating the model-based OPC edge database **1147**, the system proceeds back to step **1110** to examine another edge. After all the edges have been examined at step **1110**, the system proceeds to begin the model-based correction stage.

At step **1160**, the system applies the manufacturing model to the edge database. At step **1170**, the system tests all the evaluation points for the various edges to correct with model-based correction. If, at step **1175**, all the edges meet a defined specification then the system is done.

Otherwise, the system proceeds to step **1180** to iteratively extract each edge from the model-based edge database **1147** and apply a model based correction at step **1185**. This is performed until all the edges needing model based OPC have been adjusted. The system then again applies the manufacturing model and tests the evaluation points at steps **1160**, **1170** and **1175** to determine if the all edges are now to specification. This iterative process continues until the layout conforms to the defined specification.

Using Multiple Different Models

As set forth in the introductory section on model-based OPC, many different types of models have been created to model various semiconductor-manufacturing processes. Each model may have its own particular strenghts and weaknesses. Some models may be better than other models in certain defined circumstances.

The hybrid OPC system of the present invention may take advantage of these different models. As set forth in the previous sections, many embodiments use various rules to specify a particular correction system to be used. These rule sets may be expanded to select a particular type of OPC model that should be used to evaluate a particular feature. Thus, if a particular manufacturing model is better than other manufacturing models at modeling a particular feature, then that manufacturing model may be used to test and correct that particular feature. For example, a rule set may specify that inner corner segments should be modeled with model 1, the outer corner segments should be modeled with model 2, and the edge segments should be modeled with model 3. In this manner, the system will take advantage of the best model for each particular circum stance.

Applications Of Hybrid OPC

The hybrid OPC system of the present invention is very useful for traditional optical lithography semiconductor manufacturing. However, its application is not limited to that area. The teachings of the present invention may be used for any photo-mask based manufacturing process. For example, the teachings of the present invention may be applied to both binary masks and phase-shifting masks. Information about phase-shifting masks can be found in U.S. patent 5,858,580 issued on January 12, 1999 entitled "Phase shifting circuit manufacture method and apparatus" which is hereby incorporated by reference.

In one embodiment, the rules may be adjusted to support specialized layouts. For example, a set of rules may specify that rule-based OPC should be used to process the binary

portion of a layout and that model-based OPC should be used to process the phase-shifted portion of a layout. In this manner, the best processing is provided to those critical sections that need it the most.

Pre-Filtering

To limit the hybrid OPC system of the present invention, the software may be configured to "pre-filter" its operation. For example, a user may designate only specific areas for hybrid OPC processing. In one embodiment, the user may specify only certain cells of a layout for OPC processing. Furthermore, the type of processing to perform may be limited on a cell by cell basis. For example, certain cells may be processed with rule only OPC, other cells may be processed with model based OPC, and other cells may be processed with the hybrid OPC system. Certain features may overlap areas. For an area-based correction, the present invention may define another layer in the layout and decide that all the segments overlapped by this layer should be, corrected by a specific OPC system.

Verification Using Model Based Correction

As set forth in the previous sections, many embodiments of the present invention use model based OPC to test and set all the features in a layout design. The testing is performed using a verification specification. In such embodiments wherein all the features are tested with a verification specification, the layout is inherently fully verified by the OPC processing. Thus, no separate verification step is necessary.

To enhance the verification capabilities, the model based OPC portion of such embodiments may be improved to offer additional features sometimes available in traditional verification tools. For example, the model-based OPC portion may provide an option to test a layout design at various dose settings. This may be accomplished by adjusting the model threshold (dose). Similarly, the model-based OPC portion may provide an option to test a layout design at various focus settings. This may be accomplished by building new models at certain defocus values in order to provide focus latitude verification.

Learning Based on Model Based Correction

When performing model-based OPC, the system will perform an iterative trial and error process to adjust features (such as edge placements) in order to correct defects in a layout. However, if changes are made to a layout design, then the entire OPC process must be performed

again. Since the OPC process is a very long computationally expensive task, a simple design change may cause a long delay due to the OPC process.

To prevent such delays, the present invention introduces the idea of creating a database of changes made to a particular layout such that if a slightly changed version of the same layout is again processed, the unchanged areas can be quickly corrected using the stored database of changes. The process would simply verify that an area that was corrected in a previous OPC process has not changed such that the same correction can be applied.

In one embodiment, this correction database takes the form of a rule database. Specifically, each model-based OPC correction is stored along with the initial condition that caused the model-based OPC correction. In this manner, the set of rules can be applied to quickly bring a slightly modified design into a form where it is nearly fully corrected. The system then just applies model-based OPC to the changed areas.

An Example Embodiment

The hybrid OPC system of the present invention may be used in many different environments. **Figure 12** illustrates one example of how the hybrid OPC system may be implemented. Referring to **Figure 12**, a computer system **1200** contains a processor **1210** for executing computer instructions and a memory **1220** for storing computer programs. The hybrid OPC system of the present invention may be implemented as a hybrid OPC program **1225** that runs within the memory **1220**. The hybrid OPC program **1225** may process layout data stored within local storage device **1240**.

The hybrid OPC program **1225** may also work within a network environment. Referring to **Figure 12**, the computer system **1200** may also have a network interface **1270** that couples the computer system **1200** to a network **1275**. In such an embodiment, the hybrid OPC program **1225** may process data located on network accessible storage systems such as storage device **1277**.

The hybrid OPC program **1225** may be leased or sold to customers that wish to improve their semiconductor layouts. The hybrid OPC program **1225** may be distributed on magnetic, optical, or other computer readable media. Alternatively, the hybrid OPC program **1225** may be distributed electronically using any transmission medium such as the Internet, a data broadcast, or any other digital transmission medium.

The foregoing has described a method and apparatus for mixed-mode optical proximity correction of semiconductor circuit layouts. It is contemplated that changes and modifications may be made by one of ordinary skill in the art, to the materials and arrangements of elements of the present invention without departing from the scope of the invention.

CLAIMS

We claim:

1. A method of preparing a semiconductor mask, said method comprising:

accepting a semiconductor design;

processing said semiconductor design with a set of optical proximity correction rules to produce a rule corrected semiconductor design;

modeling said rule corrected semiconductor design with an optical model to produce a modeled semiconductor mask; and

adjusting said corrected semiconductor design to correct said modeled semiconductor mask.

2. The method as claimed in claim 1 wherein said step of modeling said rule corrected semiconductor design comprises verifying said semiconductor design against specifications.

3. The method as claimed in claim 2 wherein a user may select a dose setting for said verifying.

4. The method as claimed in claim 2 wherein a user may select a focus setting for said verifying.

5. A method of preparing a semiconductor mask, said method comprising:

accepting a semiconductor design;

processing said semiconductor design with a set of optical proximity correction rules to produce a rule corrected semiconductor design;

examining said rule-corrected semiconductor design to identify a set of features to process with model-based optical proximity correction; and

processing said set of features with model-based optical proximity correction;

outputting a final corrected semiconductor design.

6. The method as claimed in claim 5 wherein processing said set of features with model-based optical proximity correction comprises verifying said semiconductor design against specifications. .

7. The method as claimed in claim 6 wherein a user may select a dose setting for said verifying.

8. The method as claimed in claim 6 wherein a user may select a focus setting for said verifying.

9. The method as claimed in claim 5 wherein examining rule-corrected semiconductor design to identify a set of features to process with model-based optical proximity correction comprises applying a set of rules to identify difficult features.

10. The method as claimed in claim 5 wherein examining rule-corrected semiconductor design further comprises selecting a particular model-based optical proximity correction system for each feature.

11. The method as claimed in claim 5 wherein a feature comprises a segment.

12. The method as claimed in claim 5 wherein a feature comprises a shape.

13. A method of preparing a semiconductor mask, said method comprising:

accepting a semiconductor design;

processing each feature to determine if a ruled-based optical proximity correction system or a model-based optical proximity correction system should be used for a particular feature;

selectively correcting each feature with said ruled-based optical proximity correction system or said model-based optical proximity correction system; and

outputting a final corrected semiconductor design.

14 The method as claimed in claim 13 further comprising:

selecting a particular model-based optical proximity correction system from a set of model-based optical proximity correction system for each feature to be corrected with a model-based optical proximity correction system;

15. The method as claimed in claim 13 wherein said features to be corrected with said model-based optical proximity system are pre-biased before correcting with said model-based optical proximity system.

16. The method as claimed in claim 13 wherein selectively correcting a features with a model-based optical proximity correction comprises verifying said semiconductor design against specifications. .

17. The method as claimed in claim 16 wherein a user may select a dose setting for said verifying.

18. The method as claimed in claim 16 wherein a user may select a focus setting for said verifying.

19. The method as claimed in claim 13 wherein correcting a feature with said model-based optical proximity correction system further comprises:

processing said feature to determine a selected model-based optical proximity correction system from a set of model-based optical proximity correction systems; and

processing said feature with said selected model-based optical proximity correction system.

21. The method as claimed in claim 13 wherein a feature comprises a segment.

22. The method as claimed in claim 13 wherein a feature comprises a shape.

23. A method of preparing a semiconductor mask, said method comprising:

accepting a semiconductor design;

processing each feature to determine if a ruled-based optical proximity correction system, if a model-based optical proximity correction system, if both rule-based and model-based optical proximity correction systems, or if no correction system should be used for a particular feature;

selectively correcting each feature with a selected correction system determined in said step of processing; and

outputting a final corrected semiconductor design.

24 The method as claimed in claim 23 further comprising:

selecting a particular model-based optical proximity correction system from a set of model-based optical proximity correction system for each feature to be corrected with a model-based optical proximity correction system;

25. The method as claimed in claim 23 wherein said features to be corrected with said model-based optical proximity system are pre-biased before correcting with said model-based optical proximity system.

26. The method as claimed in claim 23 wherein selectively correcting a features with a model-based optical proximity correction comprises verifying said semiconductor design against specifications.

27. The method as claimed in claim 13 wherein a feature comprises a segment.

28. The method as claimed in claim 13 wherein a feature comprises a shape.

29. A method of preparing a semiconductor mask, said method comprising:
accepting a semiconductor design;
processing said semiconductor design with model-based optical proximity correction system;
storing a set of corrections made using said model-based optical proximity correction system;
modifying said semiconductor layout to create a modified layout; and
processing said modified layout using said stored set of corrections.

30. The method as claimed in claim 29 wherein said corrections are stored as a set of rules.

31. A semiconductor device, said semiconductor device created from a processed layout generated by:

processing an input layout design with a set of optical proximity correction rules to produce a rule corrected semiconductor design;

modeling said rule corrected semiconductor layout design with an optical model to produce a modeled semiconductor mask; and

adjusting said corrected semiconductor layout design to correct said modeled semiconductor mask.

32. A semiconductor device, said semiconductor device created from a processed layout generated by:

processing an initial semiconductor layout with a set of optical proximity correction rules to produce a rule corrected semiconductor layout;

examining said rule-corrected semiconductor layout to identify a set of features to process with model-based optical proximity correction; and

processing said set of features with model-based optical proximity correction;

outputting a final corrected semiconductor layout design.

33. A semiconductor device, said semiconductor device created from a processed layout generated by:

processing each feature in an input layout to determine if a ruled-based optical proximity correction system or a model-based optical proximity correction system should be used for a particular feature;

selectively correcting each feature with said ruled-based optical proximity correction system or said model-based optical proximity correction system; and

outputting a final corrected semiconductor design.

34. A computer readable medium, said computer readable medium containing computer instructions for:

processing an input layout design with a set of optical proximity correction rules to produce a rule corrected semiconductor design;

modeling said rule corrected semiconductor layout design with an optical model to produce a modeled semiconductor mask; and

adjusting said corrected semiconductor layout design to correct said modeled semiconductor mask.

35. A computer readable medium, said computer readable medium containing computer instructions for:

processing an initial semiconductor layout with a set of optical proximity correction rules to produce a rule corrected semiconductor layout;

examining said rule-corrected semiconductor layout to identify a set of features to process with model-based optical proximity correction; and

processing said set of features with model-based optical proximity correction;

outputting a final corrected semiconductor layout design.

36. A computer readable medium, said computer readable medium containing computer instructions for:

processing each feature in an input layout to determine if a ruled-based optical proximity correction system or a model-based optical proximity correction system should be used for a particular feature;

selectively correcting each feature with said ruled-based optical proximity correction system or said model-based optical proximity correction system; and

outputting a final corrected semiconductor design.

37. An electromagnetic waveform, said electromagnetic waveform carrying computer instructions for:

processing an input layout design with a set of optical proximity correction rules to produce a rule corrected semiconductor design;

modeling said rule corrected semiconductor layout design with an optical model to produce a modeled semiconductor mask; and

adjusting said corrected semiconductor layout design to correct said modeled semiconductor mask.

38. An electromagnetic waveform, said electromagnetic waveform carrying computer instructions for:

processing an initial semiconductor layout with a set of optical proximity correction rules to produce a rule corrected semiconductor layout;

examining said rule-corrected semiconductor layout to identify a set of features to process with model-based optical proximity correction; and

processing said set of features with model-based optical proximity correction;

outputting a final corrected semiconductor layout design.

39. An electromagnetic waveform, said electromagnetic waveform carrying computer instructions for:

processing each feature in an input layout to determine if a ruled-based optical proximity correction system or a model-based optical proximity correction system should be used for a particular feature;

selectively correcting each feature with said ruled-based optical proximity correction system or said model-based optical proximity correction system; and

outputting a final corrected semiconductor design.

40. An computer apparatus, said computer apparatus comprising:
a processor for processing computer instructions; and
a memory, said memory containing a set of computer instructions for
processing an input layout design with a set of optical proximity correction rules to produce a rule corrected semiconductor design,
modeling said rule corrected semiconductor layout design with an optical model to produce a modeled semiconductor mask, and
adjusting said corrected semiconductor layout design to correct said modeled semiconductor mask.

41. An computer apparatus, said computer apparatus comprising:
a processor for processing computer instructions; and
a memory, said memory containing a set of computer instructions for
processing an initial semiconductor layout with a set of optical proximity correction rules to produce a rule corrected semiconductor layout,
examining said rule-corrected semiconductor layout to identify a set of features to process with model-based optical proximity correction, and
processing said set of features with model-based optical proximity correction,
outputting a final corrected semiconductor layout design.

42. An computer apparatus, said computer apparatus comprising:
a processor for processing computer instructions; and
a memory, said memory containing a set of computer instructions for
processing each feature in an input layout to determine if a ruled-based optical proximity correction system or a model-based optical proximity correction system should be used for a particular feature,

selectively correcting each feature with said ruled-based optical proximity correction system or said model-based optical proximity correction system, and

outputting a final corrected semiconductor design.

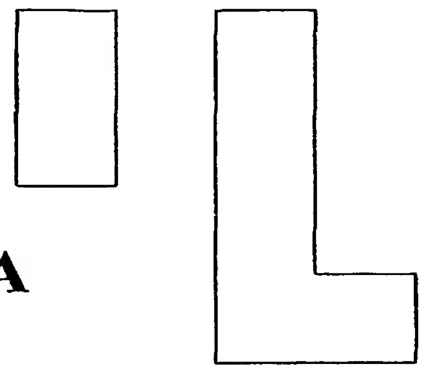


Figure 1A

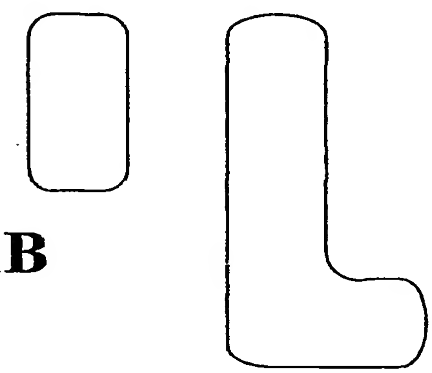


Figure 1B

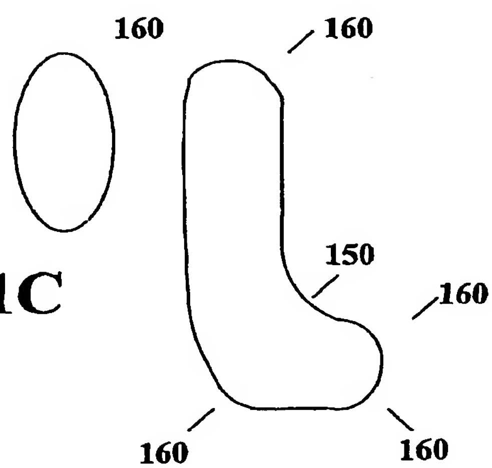


Figure 1C

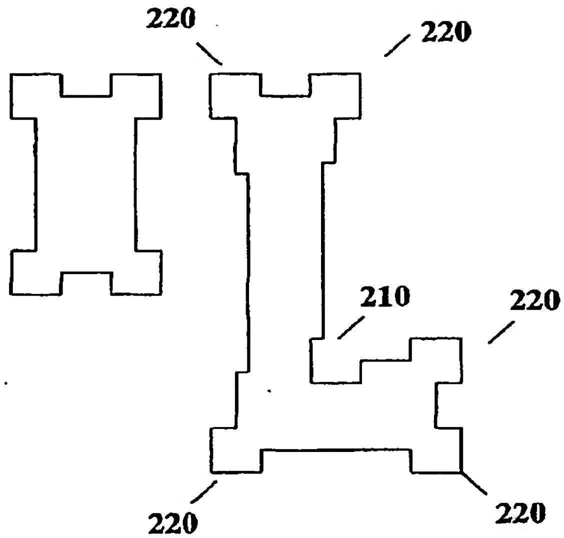


Figure 2A

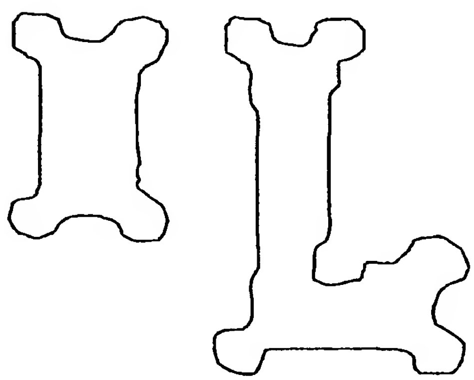


Figure 2B

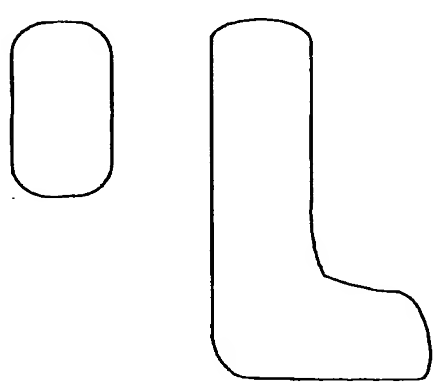


Figure 2C

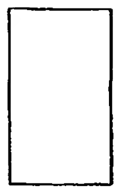


Figure 3A

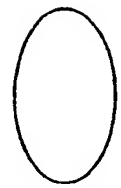


Figure 3B

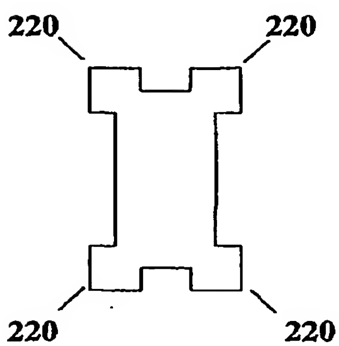


Figure 3C

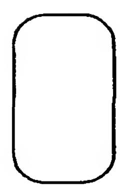


Figure 3D

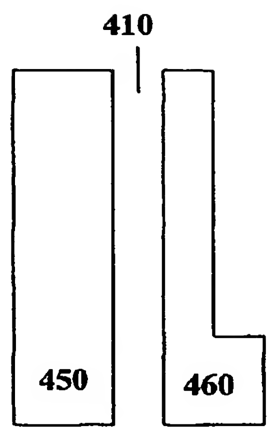


Figure 4A

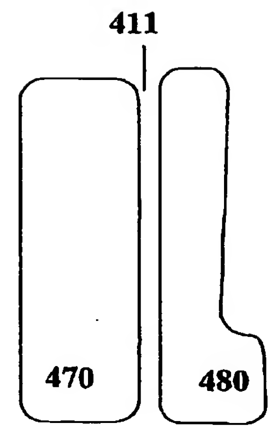


Figure 4B

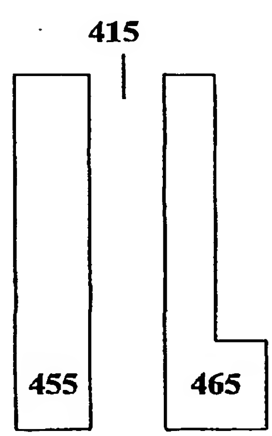


Figure 4C

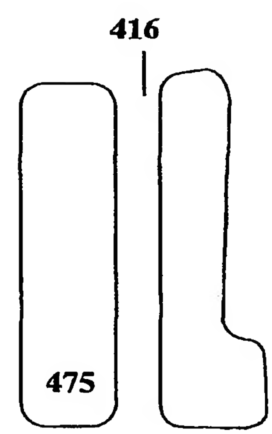


Figure 4D

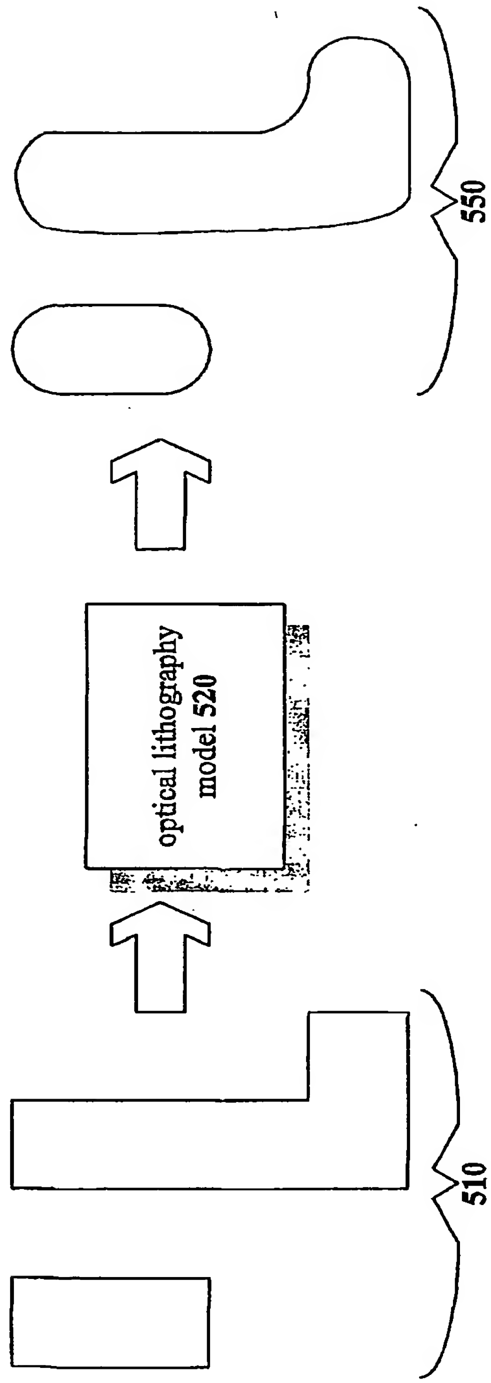


Figure 5

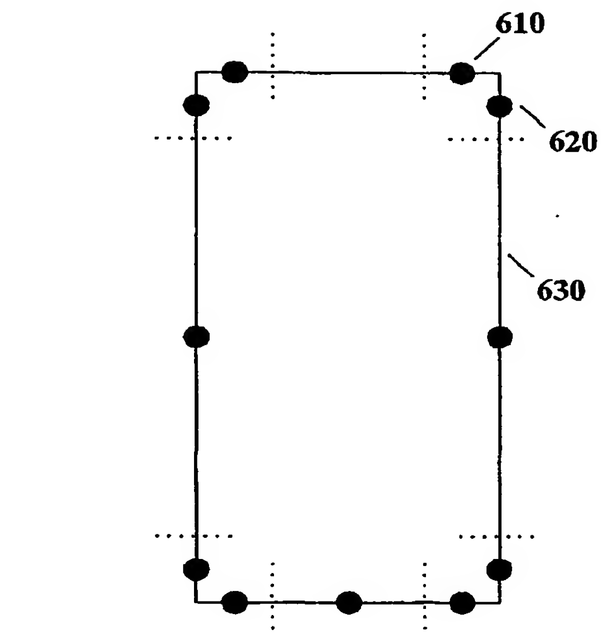


Figure 6A

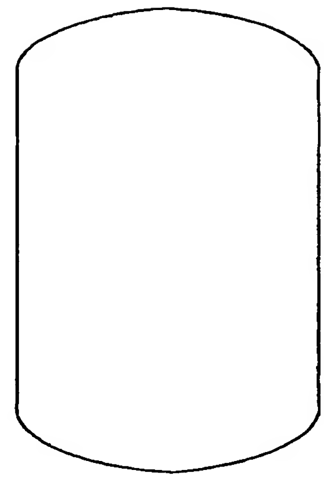


Figure 6B

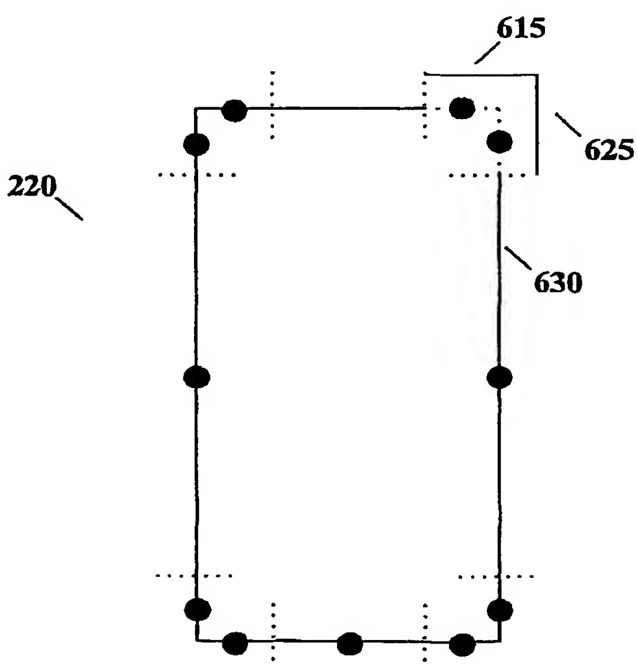


Figure 6C

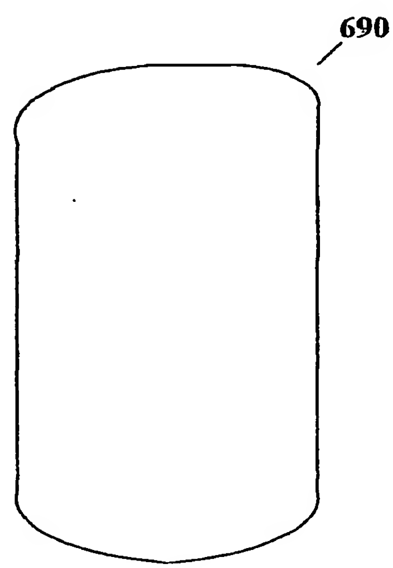


Figure 6D

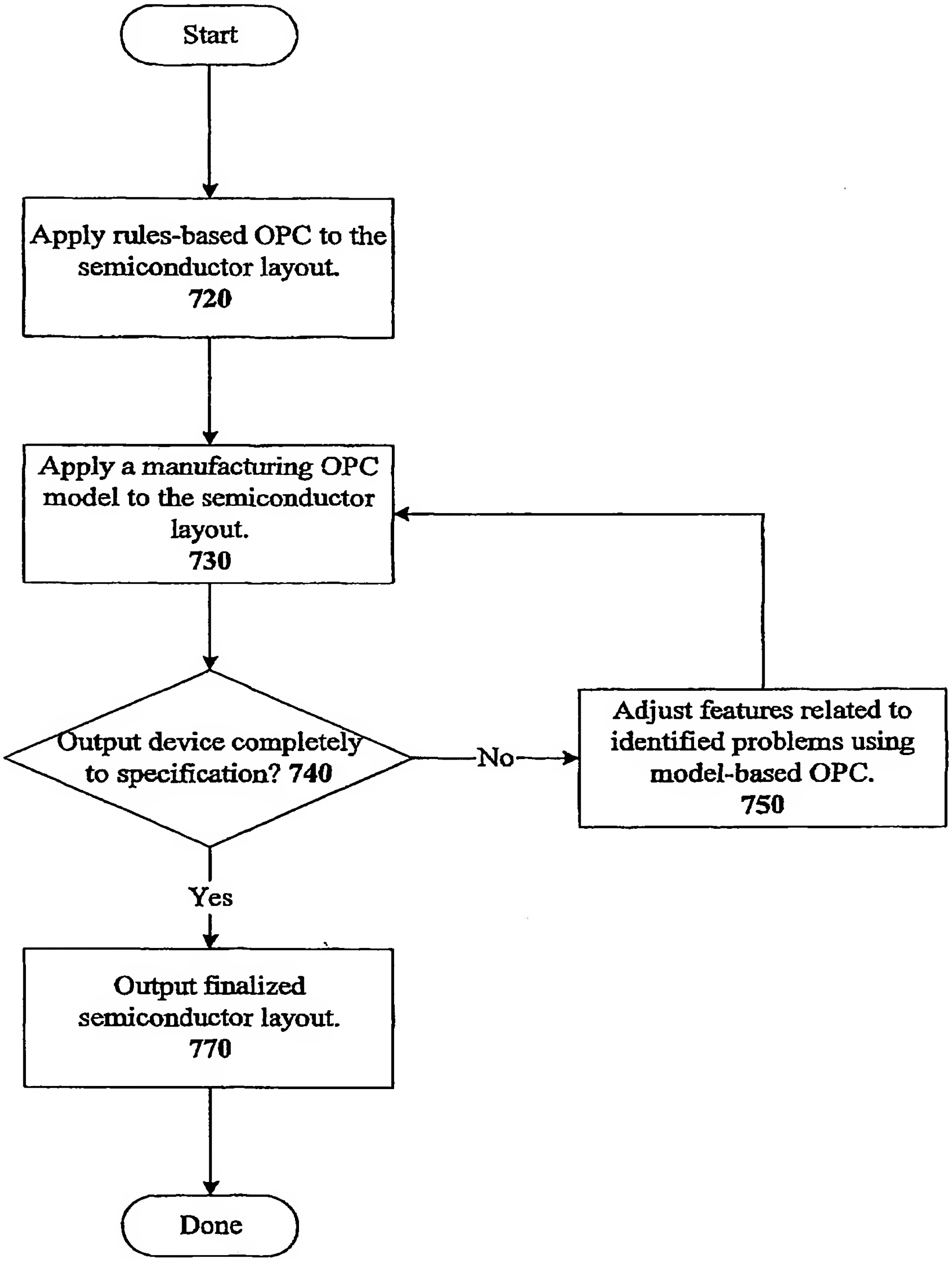

Start
Apply rules-based OPC to the semiconductor layout.
720
Apply a manufacturing OPC model to the semiconductor layout.
730
Output device completely to specification? 740
No
Adjust features related to identified problems using model-based OPC.
750
Yes
Output finalized semiconductor layout.
770
Done

Figure 7

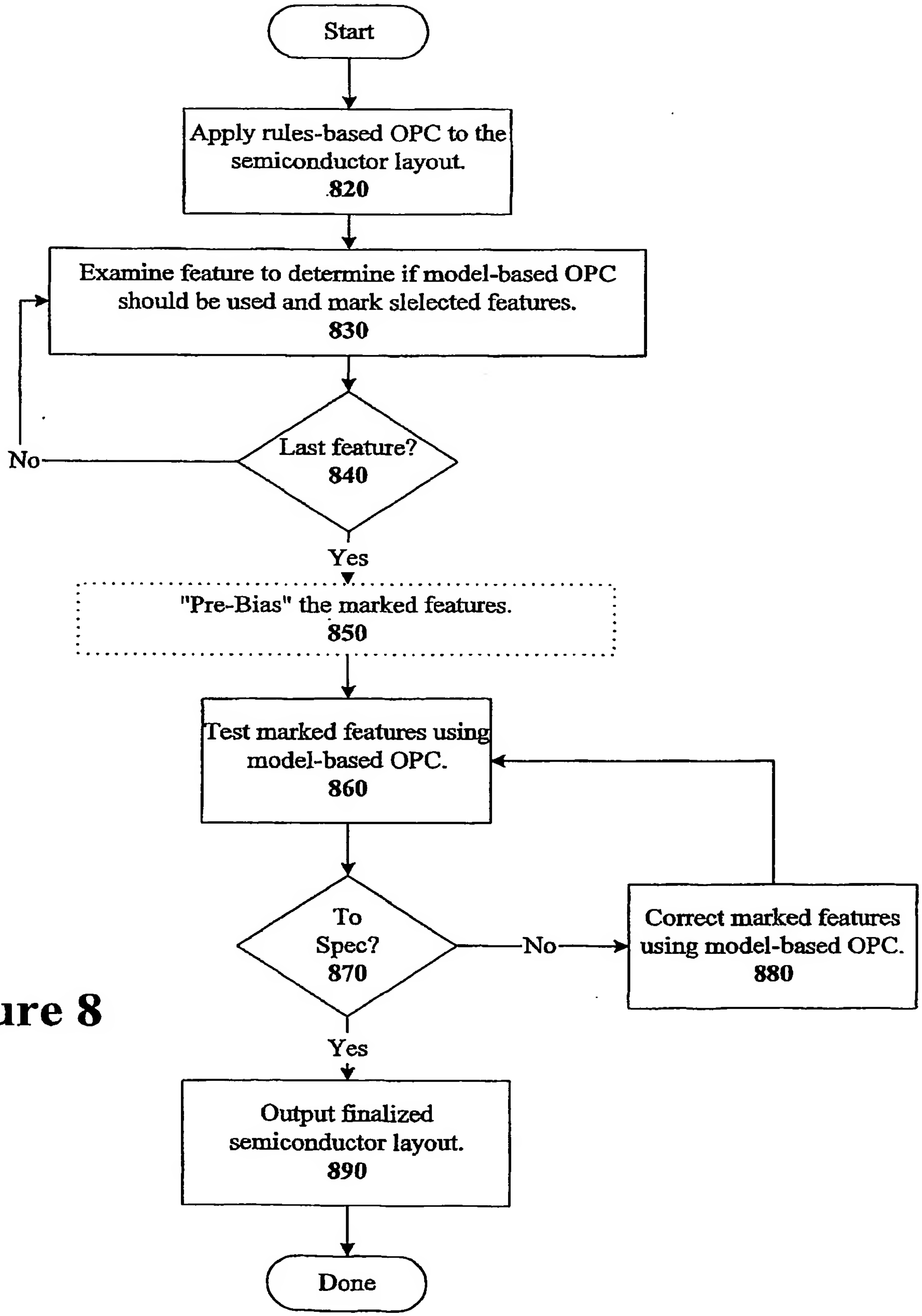

Start
Apply rules-based OPC to the semiconductor layout.
820
Examine feature to determine if model-based OPC should be used and mark slelected features.
830
Last feature?
840
No
Yes
"Pre-Bias" the marked features.
850
Test marked features using model-based OPC.
860
To Spec?
870
No
Correct marked features using model-based OPC.
880
Yes
Output finalized semiconductor layout.
890
Done

Figure 8

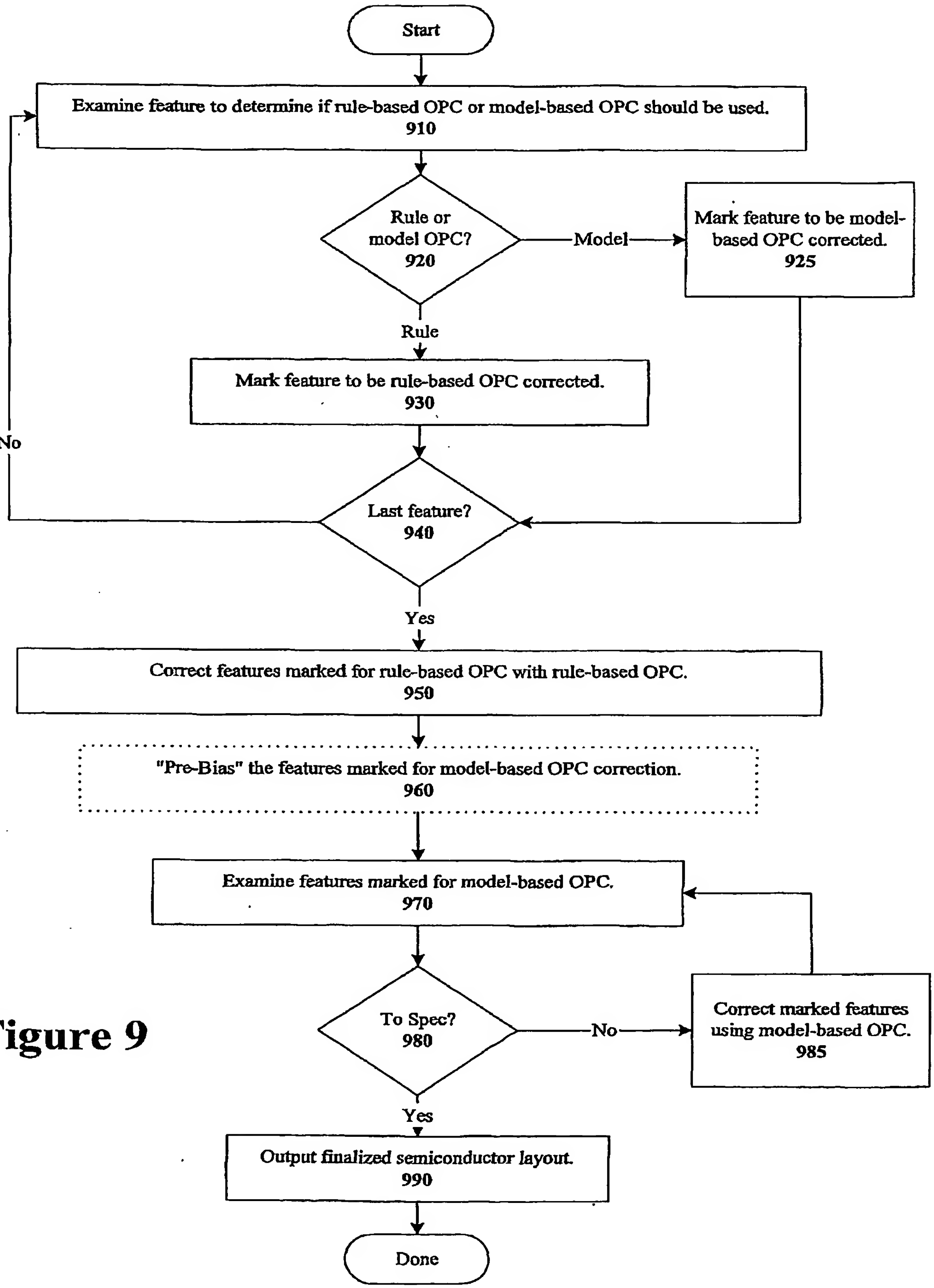

Start
Examine feature to determine if rule-based OPC or model-based OPC should be used.
910
Rule or model OPC?
920
Model
Mark feature to be model-based OPC corrected.
925
Rule
Mark feature to be rule-based OPC corrected.
930
No
Last feature?
940
Yes
Correct features marked for rule-based OPC with rule-based OPC.
950
"Pre-Bias" the features marked for model-based OPC correction.
960
Examine features marked for model-based OPC.
970
To Spec?
980
No
Correct marked features using model-based OPC.
985
Yes
Output finalized semiconductor layout.
990
Done

Figure 9

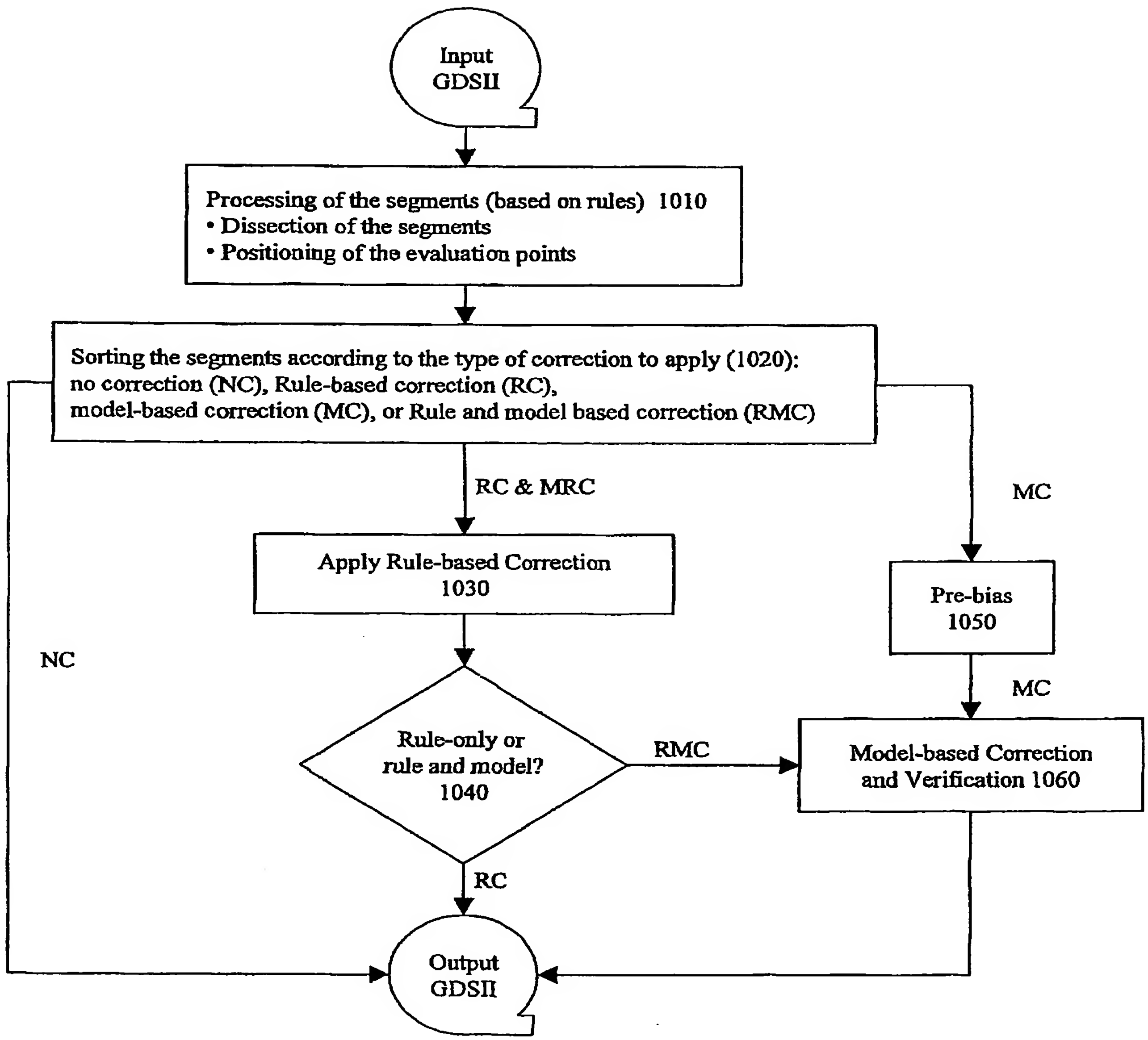

Input
GDSII
Processing of the segments (based on rules) 1010
• Dissection of the segments
• Positioning of the evaluation points
Sorting the segments according to the type of correction to apply (1020):
no correction (NC), Rule-based correction (RC),
model-based correction (MC), or Rule and model based correction (RMC)
RC & MRC
MC
Apply Rule-based Correction
1030
Pre-bias
1050
NC
MC
Rule-only or
rule and model?
1040
RMC
Model-based Correction
and Verification 1060
RC
Output
GDSII

Figure 10

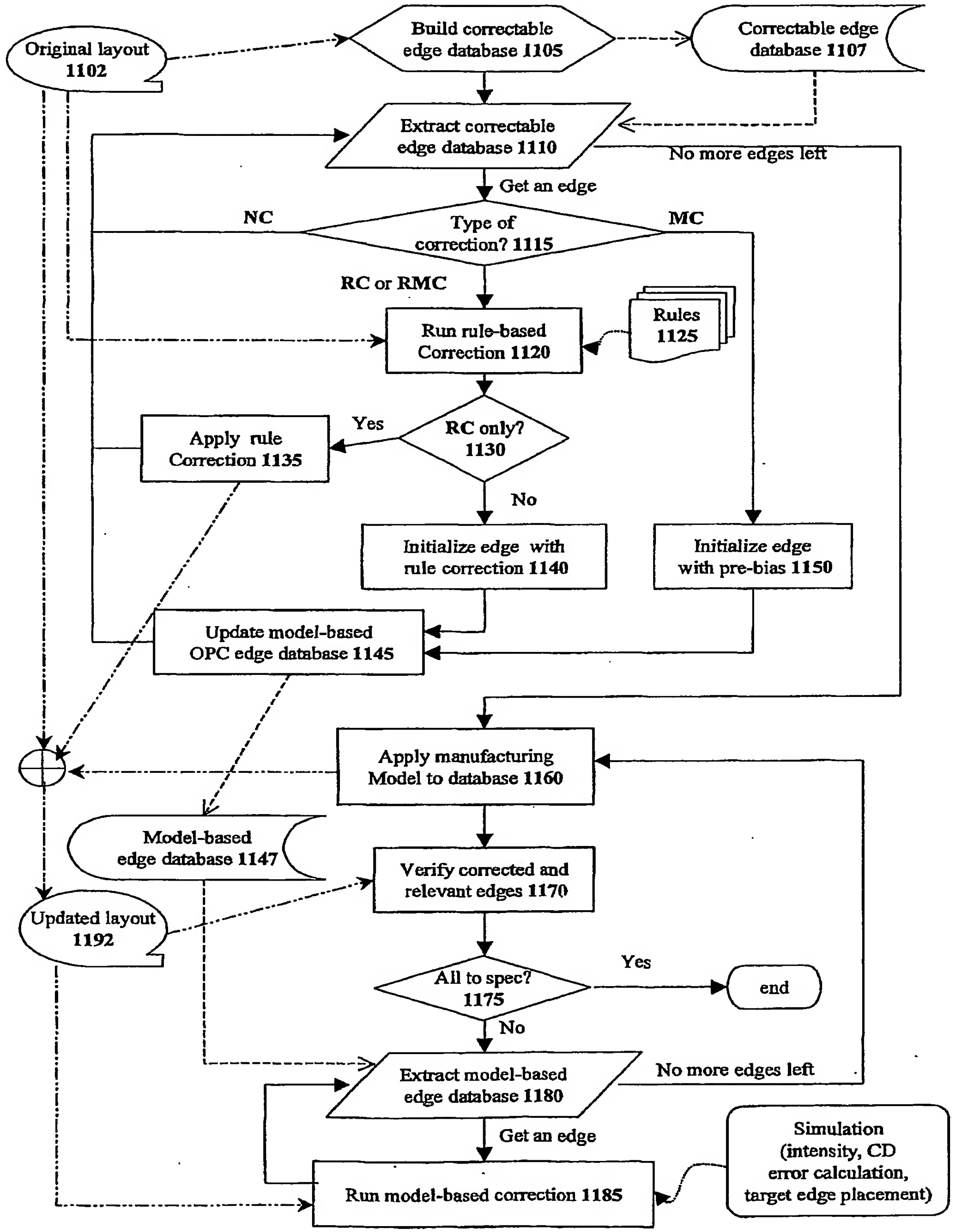
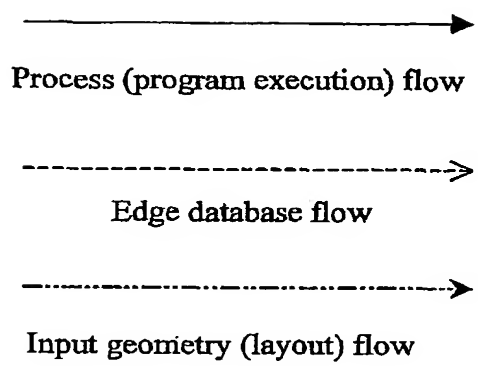

Original layout
1102
Build correctable
edge database 1105
Correctable edge
database 1107
Extract correctable
edge database 1110
No more edges left
Get an edge
NC
Type of
correction? 1115
MC
RC or RMC
Run rule-based
Correction 1120
Rules
1125
Yes
Apply rule
Correction 1135
RC only?
1130
No
Initialize edge with
rule correction 1140
Initialize edge
with pre-bias 1150
Update model-based
OPC edge database 1145
Apply manufacturing
Model to database 1160
Model-based
edge database 1147
Verify corrected and
relevant edges 1170
Updated layout
1192
Yes
All to spec?
1175
end
No
Extract model-based
edge database 1180
No more edges left
Get an edge
Simulation
(intensity, CD
error calculation,
target edge placement)
Run model-based correction 1185

Figure 11A



Process (program execution) flow
Edge database flow
Input geometry (layout) flow

Figure 11B

13/13

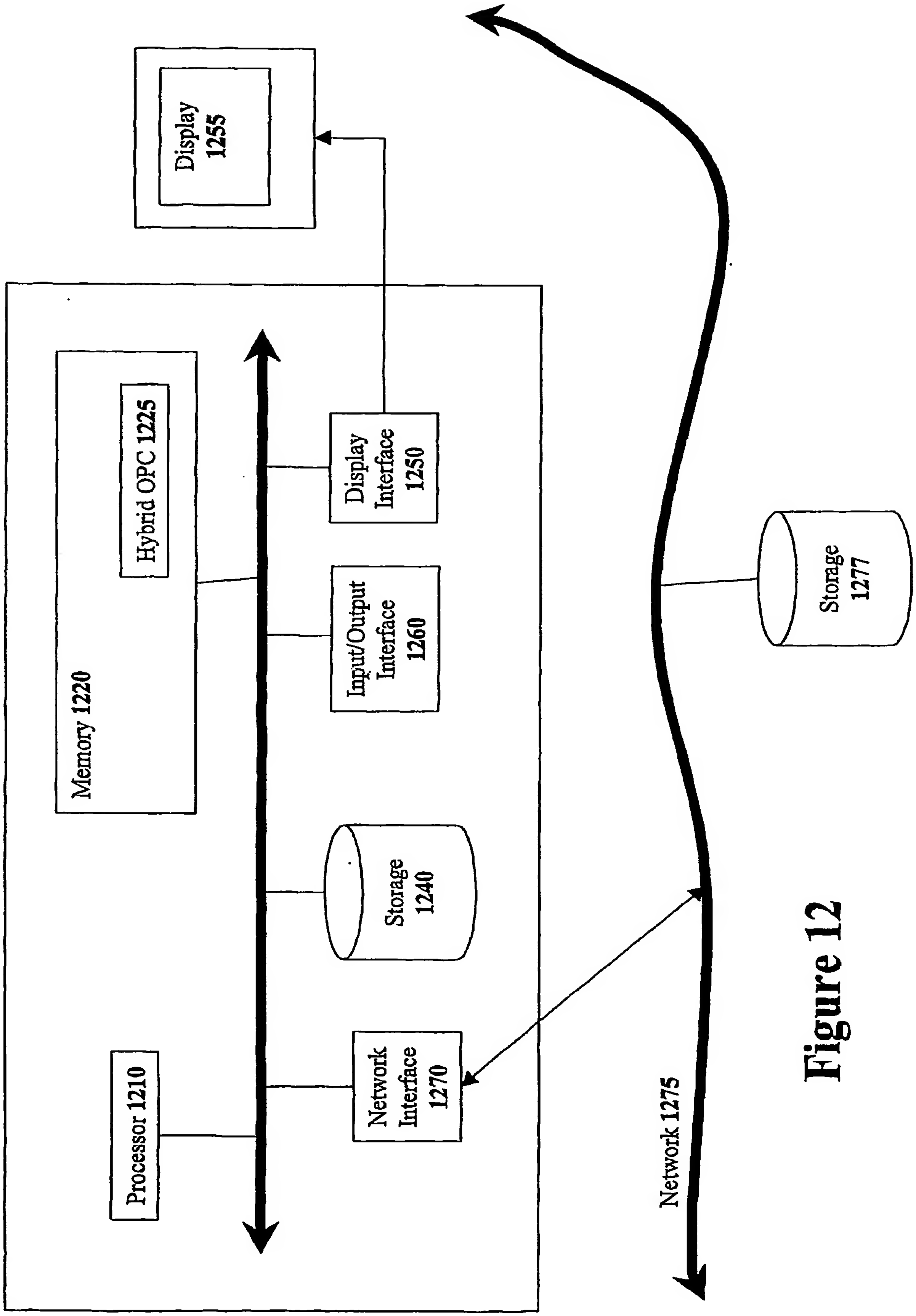


Figure 12